

# Making Device Prototype

in Yokogawa Minimal Fab Application Laboratory

## What You Can Do with Minimal Fab

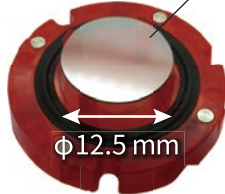
**Even special materials and expensive materials with difficulty in large diameter can be made from one piece.**

With half-inch wafers, compound semiconductor and diamond substrate can be easily fabricated from one piece.

[Results of prototype substrate]

- GaAs
- GaN
- Ga<sub>2</sub>O<sub>3</sub>
- SOI
- Glass
- Diamond
- Sapphire etc.

Diamond substrate



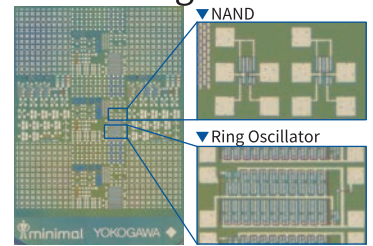
**Maskless Exposure Can Significantly Speed Up Research & Development.**

Because the direct drawing method does not require mask preparation, the prototype PDCA cycle can be performed quickly and at low cost, accelerating the development of new technologies.



For example, SOI-CMOS can be fabricated by total of 98 processes in 5 days. See the back for details.

Microscopic images of SOI-CMOS fabricated with minimal fab ▶



## Three Plans to Realize Your Ideas

**Plan 1**

Cost \$\$\$\$  
Support ●●●●●

### Prototype and Development Together

You work with process engineers in YOKOGAWA to develop the desired devices with minimal fab.

We provide prototypes with various specifications, such as materials, film thickness, film type, and structures, in consultation with you.

**Plan 2**

Cost \$\$\$\$  
Support ●●●●●

### Leave Everything to Us

Let YOKOGAWA's process engineers being well-informed on the minimal fab, make your device prototypes!

We discuss the desired device in advance with you and make prototype.

**Plan 3**

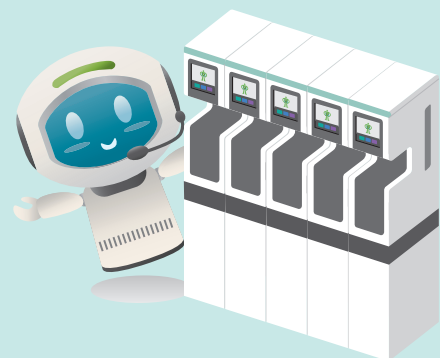
Cost \$\$\$\$  
Support ●●●●●

### Fab Rental

This plan is for the customers to make prototypes by yourselves using every facility in the Yokogawa minimal fab application laboratory.

This service is available only after receiving paid training.

**Why don't you experience the speedy device prototyping?**



# Yokogawa Minimal Fab Application Laboratory

# Tools and Results

## Outline of Tools for Prototype

### Yokogawa Minimal Fab Application Laboratory



Location: 2-9-32, Nakacho, Musashino-shi, Tokyo  
Yokogawa Electric Corporation Headquarters

### Tool List

#### [Minimal tools]

No.	Category	Tool	Process
1	Photo	Coater (1)	Resist spin coating
2		Coater (2)	Resist spin coating
3		Developer	Development
4		Maskless Exposure	Direct drawing exposure
5	Mask Aligner	Mask Aligner	Double-sided exposure
6		Focused Light Heating (1)	N-type diffusion
7		Focused Light Heating (2)	P-type diffusion
8	Heating	Oxidation Furnace	Thermal oxidation film formation
9		Laser Heating	Rapid thermal annealing and H <sub>2</sub> sintering
10	Deposition	Sputtering	Metal film deposition with 3 targets
11		TEOS PE-CVD	TEOS film deposition
12		SiN PE-CVD	SiN film deposition
13		Evaporator	High melting point metal evaporation such as Pt
14	Dry	Deep RIE	Deep Si fast etching with BOSCH process
15		CCP Etcher	Dielectric film dry etching
16		Metal Plasma Etcher	Metal film dry etching
17	Wet	Water Plasma Asher	Fast resist removal
18		RCA Station	Double-sided RCA cleaning
19		Piranha Clean	H <sub>2</sub> SO <sub>4</sub> /H <sub>2</sub> O <sub>2</sub> cleaning and organic matter removal
20		BHF Etcher	SiO <sub>2</sub> wet etching
21	Acetone-IPA Cleaner	Acetone-IPA Cleaner	Resist removal and lift-off by acetone
22		GaAs Wet Etcher	Compound semiconductor etching with H <sub>2</sub> SO <sub>4</sub> /H <sub>2</sub> O <sub>2</sub>
23	Other	SOD Doping Station	Spin coating of dopant material
24		CMP	Si and SiO <sub>2</sub> planarization
25	Measurement	Wafer Surface Scanner	Particle count on the wafer surface
26		Optical Thickness Tester	Film thickness of SiO <sub>2</sub> , SiN and resist measurement

#### [Ancillary Facilities]

No.	Category	Tool	Process
1	Work	Clean Bench	Wafer transfer into the minimal shuttle
2		Fume Hood	Local ventilation for acids, alkalis and organic solvents
3		Ultrasonic Cleaner	Ultrasonic cleaning, etc.
4	Utility	DI Water Production	DI water supply
5	Batch Processing	Sputtering	Batch process of metal sputtering with single target
6		Heating Furnace	Batch process of thermal oxidation
7	Utility	Optical Microscope	BF, DF, DIC mode and capturing entire wafer with tiling
8		Electronic Balance	It can measure up to 5 digits to the decimal point.
9		Parameter Analyzer	Electrical properties measurement
10		Prober	Electrical properties measurement
11		High Speed Camera	Motion analysis of fast rotating devices
12		Contact Angle Meter	Contact angle and surface free energy measurement
13		AFM	Surface roughness and minute step measurement
14		Surface Profiler	Step height measurement
15		SEM	High resolution observation
16		Vibration Monitor	Vibration measurement

## Results of Prototypes

### SOI-CMOS

#### Characteristics

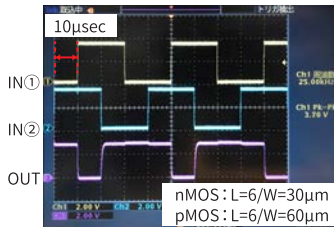
- Using SOI substrate and only minimal tools, it takes about 5 days to complete the device fabrication.
- It combines legacy processes such as thermal diffusion with advanced process technologies such as TiN gate electrode and 6nm gate oxide.

#### Result of a Prototype

- 2-input NAND with gate length of 6 μm was operated by switching the 10 μsec signal.
- 21-stage ring oscillator with gate length of 4 μm was oscillated at about 3.6 MHz.
- It is expected to be used in small-scale and highly customizable logic circuits.

#### 2-input NAND operation waveform

(V<sub>dd</sub>=3.3V, IN①·②=3.3V)

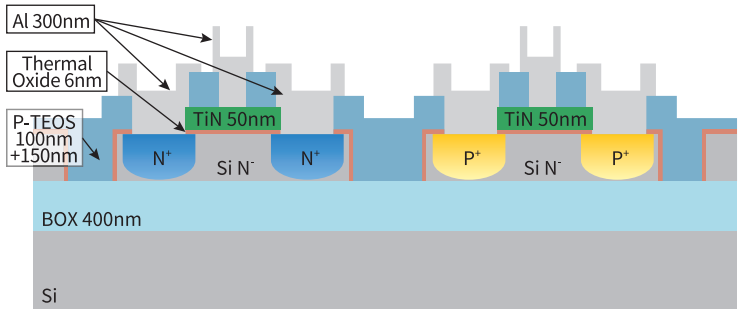


#### 21-stage Ring Oscillator operation waveform

(nMOS: L=4/W=14 μm / pMOS: L=4/W=28 μm)



#### Cross section of SOI-CMOS transistor



### Diaphragm Type MEMS Pressure Sensor

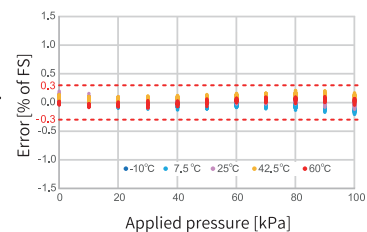
#### Characteristics

- Most of the front-end process was fabricated with minimal fab. (No.1, 3, 4, 5, 7, 9, 10, 11, 14, 19, 20, 21, 23, +1 tool)
- The completed chips were packaged and evaluated.

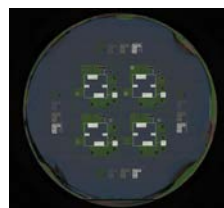
#### Result of a Prototype

- The measurement error was within 0.5%. (Measuring range: -10 to 60 °C, at pressure of 0 to 100 kPa)
- MEMS pressure sensor fab has been completed with minimal.
- The results showed the applicability of minimal fab for various MEMS applications.

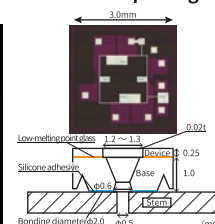
#### Pressure measurement error



#### Appearance of the completed wafer



#### Cross section of the package



#### Appearance during the evaluation

